WHAT IS CLAIMED IS:

1. A parallel-to-serial conversion device, comprising:

a voltage output device to produce a voltage representative of a value of a bit in a serial bit datastream converted from a parallel bit utilizing a combined current, the combined current divided into a first current and a second current;

n number of selection devices to accept as input n number of parallel bits, wherein an active selection device accepts as input the first current and outputs an active selection device current directly to a corresponding current source and (n – 1) non-active selection devices are inactive at one time;

a current steering device, to accept as input the second current, and outputs (n – 1) non-active selection device currents to (n – 1) number of current sources, wherein n number of current sources, each corresponding to the n number of selection devices, accepts as input the active selection device current and the (n – 1) non-active selection device currents.

2. The conversion device of claim 1, wherein n number of clock signals identify which of the n number of selection devices is actively converting.

3. The conversion device of claim 1, wherein n is equal to eight.

4. The conversion device of claim 1, wherein n is equal to ten.

5. The conversion device of claim 1, the current steering device having:

a second terminal of a first transistor and a first terminal of a second transistor coupled to a first differential node of the voltage output device;

a second terminal of the second transistor and a first terminal of the first transistor coupled to a second differential node of the voltage output device; and

a third terminal of the first transistor and the second transistor coupled to the (n – 1) non-active selection devices.

6. A method of converting n parallel bits one at a time to a bit in a serial bit datastream in a current efficient manner, comprising:

inputting n parallel bits to n number of selection devices;

identifying one of the n number of selection devices as an active selection device and (n – 1) number of selection devices as inactive selection devices;

dividing an output current into a first current and a second current;

directing the first current to the active selection device

directly coupling the active selection device to one of n number of current sources;

directing the second current to a current steering device;

coupling the current steering device to (n – 1) current sources corresponding to the (n – 1) inactive selection devices; and

converting an active parallel bit input via the active selection device to the bit in the serial datastream by generating a voltage representative of a value of the bit utilizing a combined current from the n current sources.

7. The method of claim 6, wherein n number of clock signals identify the active selection device.

8. The method of claim 6, wherein n is equal to eight.

9. The method of claim 6, wherein n is equal to ten.

10. The method of claim 6, wherein the current steering device and the inactive selection devices allow the control of output by the input data bit or latch on a previous data bit

if there is no input, namely the current steering device allows a differential current to flow in either direction.

11. A transmitting device, comprising:

a parallel-to-serial converter to convert n parallel bits one at a time to a bit in a serial bit datastream having:

a voltage output device to produce a voltage representative of a value of a bit in a serial bit datastream converted from a parallel bit utilizing a combined current, the combined current divided into a first current and a second current;

n number of selection devices to accept as input n number of parallel bits, wherein an active selection device accepts as input the first current and outputs an active selection device current directly to a corresponding current source and (n – 1) non-active selection devices are inactive at one time;

a current steering device, to accept as input the second current, and outputs (n – 1) non-active selection device currents to (n – 1) number of current sources, wherein n number of current sources, each corresponding to the n number of selection devices, accepts as input the active selection device current and the (n – 1) non-active selection device currents; and

an output buffer to receive the serial bit in the serial bit datastream from the parallel-to-serial converter and to transmit a differential datastream over a transmission line.

12. The transmitting device of claim 11, further including an equalizer to receive an encoded parallel signal and to output n parallel bits in the parallel bit datastream compensated for channel frequency response to the parallel-to-serial converter.

13. The transmitting device of claim 11, wherein the current steering device and the inactive selection devices allow the control of output by the input data bit or latch on a previous data bit if there is no input, namely the current steering device allows a differential current to flow in either direction.

14. The transmitting device of claim 11, wherein n number of clock signals determine the active selection device.

15. The transmitting device of claim 11, wherein n is equal to ten.

16. The transmitting device of claim 11, wherein n is equal to eight.

17. The transmitting device of claim 11, where the transmitting device is a 10 Gigabit per second Media Independent Interface (XGMII)-to-10 Gigabit per second Attachment Unit Interface (XAUI) transmitting device.

18. The transmitting device of claim 11, the current steering device having:

a second terminal of a first transistor and a first terminal of a second transistor coupled to a first differential node of the voltage output device;

a second terminal of the second transistor and a first terminal of the first transistor coupled to a second differential node of the voltage output device; and

a third terminal of the first transistor and the second transistor connected to the (n – 1) non-active selection devices.